AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming ~~an insulating film~~ sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

forming a resist over the conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the conductive film by using the resist mask so that a portion of the sidewalls is exposed; and

etching a ~~part~~ portion of the etched conductive film to form source and drain electrodes which are in contact with the source and drain regions.

2. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming ~~an insulating film~~ sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

forming a resist over the conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the conductive film by using the resist mask; and

etching a ~~part~~ portion of the etched conductive film and a ~~part~~ portion of ~~the semiconductor region~~ the source and drain regions to form source and drain electrodes which are in contact with the source and drain regions.

3. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

etching a ~~part~~ portion of the conductive film;

forming a resist over the conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the conductive

film, said upper surface being located over the gate electrode, thereby leaving a resist mask; and

etching a ~~part~~ portion of the conductive film by using the resist mask to form source and drain electrodes which are in contact with the source and drain regions.

4. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

etching a ~~part~~ portion of the conductive film and a ~~part~~ portion of ~~the semiconductor region~~ the source and drain regions;

forming a resist over the conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask; and

etching a ~~part~~ portion of the conductive film by using the resist mask to form source and drain electrodes which are in contact with the source and drain regions.

5. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a first insulating film over a semiconductor region including source and drain regions;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode;

forming a third insulating film over the semiconductor region;

etching the third insulating film to form [[a]] sidewalls covering at least sides of the gate electrode;

etching the first insulating film by using the sidewalls and the hard mask as a mask to form a gate insulating film and to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a second conductive film;

forming a resist over the second conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the second conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the second conductive film by using the resist mask as a mask so that a portion of the sidewalls is exposed; and

etching a ~~part~~ portion of the etched second conductive film and a ~~part~~ portion of the semiconductor region to form a source and drain electrode.

6. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a first insulating film over a semiconductor region including source and drain regions;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode;

forming a third insulating film over the semiconductor region;

etching the third insulating film to form [[a]] sidewalls covering at least sides of the gate electrode;

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film and to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a second conductive film;

etching a ~~part~~ portion of the second conductive film;

forming a resist over the second conductive film;

removing ~~a portion of the resist by etching an entire surface of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the second conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask; and

etching a ~~part~~ portion of the second conductive film by using the resist mask as a mask to form a source and drain electrode.

7. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 1, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

8. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 1, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a ~~part~~ portion of the conductive film.

9. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 1, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

10. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 9, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

11. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 9, wherein the semiconductor thin film is a crystalline silicon film.

12. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 2, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

13. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 2, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a ~~part~~ portion of the conductive film.

14. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 2, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

15. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 14, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

16. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 14, wherein the semiconductor thin film is a crystalline silicon film.

17. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 3, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

18. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 3, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a ~~part~~ portion of the conductive film.

19. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 3, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

20. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 19, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

21. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 19, wherein the semiconductor thin film is a crystalline silicon film.

22. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 4, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

23. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 4, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a ~~part~~ portion of the conductive film.

24. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 4, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

25. (Currently Amended l) A method for manufacturing a semiconductor ~~element~~ device according to Claim 24, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

26. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 24, wherein the semiconductor thin film is a crystalline silicon film.

27. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 5, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

28. Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 5, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a ~~part~~ portion of the second conductive film.

29. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 5, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

30. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 29, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

31. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 29, wherein the semiconductor thin film is a crystalline silicon film.

32. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 6, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

33. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 6, wherein the resist mask is formed by removing a portion of the

resist over a channel forming region, and exposing a ~~part~~ portion of the second conductive film.

34. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 6, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

35. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 34, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

36. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 34, wherein the semiconductor thin film is a crystalline silicon film.

Claims 37-56 (Canceled)

57. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming an insulating film covering at least sides of the gate electrode;

etching a portion of the insulating film to expose a ~~part~~ portion of the semiconductor region and to form portions of the insulating film remaining on at least side surfaces of the gate electrode;

etching the gate insulating film by using the remaining portion of the insulating film as a mask to expose an upper surface of the source and drain regions;

forming a conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

forming a resist over the conductive film;

removing ~~a portion of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the conductive film by using the resist mask so that a portion of the remaining portion of the insulating film is exposed; and

etching a ~~part~~ portion of the etched conductive film to form source and drain electrodes which are in contact with the source and drain regions, and

wherein ~~said part of the semiconductor region is~~ the source and drain regions are outside of the remaining portion of the insulating film, and

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of ~~the semiconductor region~~ the source and drain regions.

58. Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 57, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

59. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 57, wherein the resist mask is formed by etching an entire face of the resist, and exposing a ~~part~~ portion of the conductive film.

60. (Currently Amended) A method for manufacturing a semiconductor element according to Claim 57, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

61. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 60, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

62. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 60, wherein the semiconductor thin film is a crystalline silicon film.

Claim 63 (Canceled)

64. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming ~~an insulating film~~ sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a first conductive film over the semiconductor region after exposing the ~~parts of the semiconductor region~~ source and drain regions;

forming a resist over the first conductive film;

removing ~~a portion of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the first conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the first conductive film by using the resist mask to form a second conductive film; and

etching a ~~part~~ portion of the second conductive film to form a source electrode and a drain electrode ,

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of ~~the semiconductor region~~ the source and drain regions.

65. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 64, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

66. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 64, wherein the resist mask is formed by etching an entire face of the resist, and exposing a ~~part~~ portion of the conductive film.

67. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 64, wherein the semiconductor region is a semiconductor thin film.

68. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 67, wherein the semiconductor thin film is a crystalline silicon film.

Claim 69 (Canceled)

70. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device comprising steps of:

forming a gate insulating film over a semiconductor region including source and drain regions;

forming a gate electrode over the semiconductor region with the gate insulating film interposed therebetween;

forming ~~an insulating film~~ sidewalls covering at least sides of the gate electrode;

etching the gate insulating film by using the sidewalls as a mask to expose an upper surface of the source and drain regions;

~~exposing a part of the semiconductor region;~~

forming a first conductive film over the semiconductor region after exposing ~~a part of the semiconductor region~~ the source and drain regions;

forming a resist over the first conductive film;

removing ~~a portion of the resist to form a resist mask~~ an entire upper portion of the resist to expose an upper surface of the first conductive film, said upper surface being located over the gate electrode, thereby leaving a resist mask;

etching a ~~part~~ portion of the first conductive film by using the resist mask to form a second conductive film;

etching a ~~part~~ portion of the second conductive film to form a source electrode and a drain electrode,

forming an interlayer insulating film over the source electrode and the drain electrode, and

forming at least one connection wiring over the interlayer insulating film,

wherein said connection wiring is connected to one of the source electrode and the drain electrode through a hole of the interlayer insulating film , and

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of ~~the semiconductor region~~ the source and drain regions.

71. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 70, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.

72. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 70, wherein the resist mask is formed by etching an entire face of the resist, and exposing a ~~part~~ portion of the conductive film.

73. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 70, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

74. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 73, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate.

75. (Currently Amended) A method for manufacturing a semiconductor ~~element~~ device according to Claim 73, wherein the semiconductor thin film is a crystalline silicon film.

Claim 76 (Canceled)